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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,443	11/27/2001	Brian D. Herr	POU920010125US1	9512

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EXAMINER	
PEUGH, BRIAN R	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,443	HERR ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,14 and 22* is/are allowed.

6)☒ Claim(s) *1-6,8-13,15-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed December 28, 2004 in response to PTO Office Action dated September 30, 2004. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-22 have been presented for examination in this application. In response to the last Office Action, claims 1-6, 8-13, and 15-21 have been amended.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8-13, and 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goldstein et al. (US# 6,247,105) in view of Yarborough (US# 6,226,725).

Regarding claim 1, Goldstein et al. teaches implementing memory allocation in a **time sensitive data communications** system according to the computer system in

which the invention is implemented, where the computer system includes I/O devices such as serial and parallel communication ports, network interfaces, etc. (Fig. 3; col. 9, lines 48-59). Allocatable memory space is divided into multiple **base memory blocks**, where each of these memory blocks comprises a number of pages, and each page comprises a number of buckets. A bucket comprises a unit of memory space that may be allocated **(pinned)** (col. 4, lines 38-42 & 46-51; col. 5, lines 12-17). Figures 2 and 4 illustrate the memory allocation system of Goldstein et al. The **base memory block** refers to a memory page that is selected, which contains the optimum number of free buckets according to a memory request. This means that a request for a section of memory is made according to the desired bucket size (**specification of buffer size**) (col. 10, lines 40-45). The **memory buffer** as claimed refers to a size of memory space to be used for a process, which may or may not be greater than the size of a single bucket allocated from memory. At step 404, the system of Goldstein et al. **determines whether a sufficient amount of memory** has been allocated for the request (col. 10, lines 46-54), in that it is determined whether the allocated bucket is large enough to satisfy the memory request according to the request's size. If additional memory space is required, another bucket of the **same size** as the bucket already allocated is **additionally allocated** from the same memory page (col. 10, lines 53-65), or from an additional memory page (col. 10, line 66 – col. 11, line 3). Goldstein et al. **does not teach that the additionally allocated memory must be contiguous** with the previously allocated memory.

Regarding claims 2, 9, and 17, Goldstein et al. teaches that all memory blocks, and thus pages and buckets (**buffers**), are stored in the memory space. The memory space is run by the memory space allocator (**kernel memory allocation module**) and prevents other processes from using or modifying the memory space (**pinning**) (col. 4, lines 38-42).

Regarding claims 3, 11, and 18, free (**additional pinned kernel memory blocks**) buckets for allocation are linked according to a **linked list** found in the descriptor block of the memory page (col. 7, lines 52-60).

Regarding claims 4, 12, and 19, each memory page contains buckets of a certain size according to the memory block to which the page is allocated. Each bucket within that block are of the **same predetermined size** (Figure 1; col. 5, lines 12-18).

Regarding claims 5, 13, and 20, Goldstein et al. teaches that the invention may be implemented for use in the general purpose computer system of Figure 3, or that the invention may be implemented to function in any type of computer system or programming or processing environment (col. 9, lines 29-30; col. 10, lines 10-12), which read upon the **mass storage data server application processing module** as claimed.

Regarding claims 6, 15, and 21, the claim limitations do not state or require that the first memory buffer is still allocated to the base memory block and additional

memory block, in that the subsequent *request* immediately follows the original *request*. Thus, these two blocks may have been released for future memory allocation after their original purpose had been satisfied and are currently empty and free for allocation. Also, the allocation of a second additional memory block (bucket) as recited in claim 6 is merely an extension of the original allocation of a first additional memory block as outlined above in regards to claim 1. The invention of Goldstein et al. teaches that if an additional bucket is not enough to satisfy the memory request, additional buckets may be allocated for the memory request according to the loop description of Figure 4 (steps 403-405). Therefore, Goldstein et al. teaches that additional buckets may be allocated in accordance to the size of the requested buffer, or memory request.

Regarding claim 8, Goldstein et al. teaches implementing memory allocation in a **time sensitive data communications** system according to the computer system in which the invention is implemented, where the computer system includes I/O devices such as serial and parallel communication ports, network interfaces, etc. (Fig. 3; col. 9, lines 48-59). The operating system **kernel (memory allocation module)** reserves the **kernel memory** area for exclusive use by the kernel (col. 4, lines 38-42). Allocatable memory space is divided into multiple **base memory blocks**, where each of these memory blocks comprises a number of pages, and each page comprises a number of buckets. A bucket comprises a unit of memory space that may be allocated (col. 4, lines 38-42 & 46-51; col. 5, lines 12-17). Figures 2 and 4 illustrate the memory allocation system of Goldstein et al. The **base memory block** refers to a memory page that is selected, which contains the optimum number of free buckets according to a

memory request. This means that a request for a section of memory is made according to the desired bucket size (**specification of buffer size**) (col. 10, lines 40-45). The **memory buffer** as claimed refers to a size of memory space to be used for a process, which may or may not be greater than the size of a single bucket allocated from memory. At step 404, the system of Goldstein et al. **determines whether a sufficient amount of memory** has been allocated for the request (col. 10, lines 46-54), in that it is determined whether the allocated bucket is large enough to satisfy the memory request according to the request's size. If additional memory space is required, another bucket of the **same size** as the bucket already allocated is **additionally allocated** from the same memory page (col. 10, lines 53-65), or from an additional memory page (col. 10, line 66 – col. 11, line 3). Goldstein et al. **does not teach that the additionally allocated memory must be contiguous** with the previously allocated memory.

Regarding claim 10, and as seen in Figure 2, the allocatable free buckets are **not found contiguously** (col. 7, lines 60-67).

Regarding claim 16, Goldstein et al. teaches implementing memory allocation in a **time sensitive data communications** system according to the computer system in which the invention is implemented, where the computer system includes I/O devices such as serial and parallel communication ports, network interfaces, etc. (Fig. 3; col. 9, lines 48-59). The operating system kernel reserves the **kernel memory** area for exclusive use by the kernel (col. 4, lines 38-42). As is notoriously well known in the art,

the kernel is comprised of **computer instructions** that provide the backbone of an operating system, all of which are inherently **stored on a storage medium**, such as a hard disk drive. Allocatable memory space is divided into multiple **base memory blocks**, where each of these memory blocks comprises a number of pages, and each page comprises a number of buckets. A bucket comprises a unit of memory space that may be allocated (col. 4, lines 38-42 & 46-51; col. 5, lines 12-17). Figures 2 and 4 illustrate the memory allocation system of Goldstein et al. The **base memory block** refers to a memory page that is selected, which contains the optimum number of free buckets according to a memory request. This means that a request for a section of memory is made according to the desired bucket size (**specification of buffer size**) (col. 10, lines 40-45). The **memory buffer** as claimed refers to a size of memory space to be used for a process, which may or may not be greater than the size of a single bucket allocated from memory. At step 404, the system of Goldstein et al. **determines whether a sufficient amount of memory** has been allocated for the request (col. 10, lines 46-54), in that it is determined whether the allocated bucket is large enough to satisfy the memory request according to the request's size. If additional memory space is required, another bucket of the **same size** as the bucket already allocated is **additionally allocated** from the same memory page (col. 10, lines 53-65), or from an additional memory page (col. 10, line 66 – col. 11, line 3). Goldstein et al. **does not teach that the additionally allocated memory must be contiguous** with the previously allocated memory.

Regarding the amended portions of claims 1-6, 8-13, and 15-21, Goldstein et al. teaches that allocating memory within a page boundary reduces the potential for paging errors (swapping memory pages between memory and disk) [col. 10, lines 56-59]. The difference between the claimed subject matter and that of Goldstein et al., disclosed supra is that Goldstein et al. does not recite preventing the paging out of kernel pages to disk, meaning that Goldstein et al. does not teach a non-pageable kernel memory system. Yarborough teaches that when kernel memory is pinned, the memory will not be swapped into and out of the disk, thus rendering the **kernel memory** space **as non-pageable** [col. 1, lines 27-37, 55-66; col. 2, lines 2-4]. Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Goldstein et al. and Yarborough before him at the time the invention was made to modify the kernel memory pinning system of Goldstein et al. to include the non-paging system of Yarborough, because then performance degradation due to page faulting can be avoided, as taught by Yarborough [col. 1, lines 63-65].

Allowable Subject Matter

Claims 7, 14, and 22 are allowable over the prior art of record.

Response to Arguments

Applicant's arguments with respect to claims 1-6, 8-13, and 15-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian R. Peugh
Patent Examiner
Art Unit 2187
March 1, 2005